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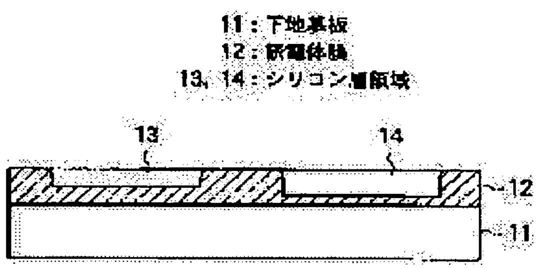
(54) SEMICONDUCTOR SUBSTRATE, MANUFACTURING METHOD THEREOF SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To enable the gates of a full depletion MOS transistor and a partial depletion MOS transistor to be very accurately formed on an SOI substrate.
SOLUTION: An SOI substrate is equipped with a base substrate 11 and a dielectric film 12 laminated on the base substrate 11, and silicon layer regions 13 and 14 different from each other in thickness are formed on the dielectric film 12. The surfaces of the silicon layer regions 13 and 14 are flush with each other. Therefore, the gate electrodes of the silicon layer regions 13 and 14 can be set equal in height to each other, a resist layer to apply can be set uniform in thickness, and the gates of accurate lengths can be formed.



本発明の第1の実施形態のSOI基板

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CLAIMS

[Claim(s)]
[Claim 1] It is the semi-conductor substrate characterized by making the front face of each of this silicon layer field into the same height while said silicon layer forms two or more silicon layer fields with at least two or more kinds of different thickness in the semi-conductor substrate which has the silicon layer insulated from the substrate substrate with the dielectric film and insulating electrically between this each silicon layer field.
[Claim 2] Between said each silicon layer field, it is the semi-conductor substrate according to claim 1 characterized by insulating by being filled up with said dielectric.
[Claim 3] Said each silicon layer field is a semi-conductor substrate according to claim 1 characterized by dissociating and forming on said dielectric film.
[Claim 4] Said each silicon layer field is a semi-conductor substrate according to claim 1, 2, or 3 characterized by having the area which can form at least two or more components, respectively.
[Claim 5] The inside of the silicon layer field of two or more kinds of said thickness on a semi-conductor substrate according to claim 1, 2, 3, or 4, The circuit which used perfect depletion mold MOS transistor or this perfect depletion mold MOS transistor is formed in the thin silicon layer field of thickness. The semiconductor integrated circuit characterized by forming in the thick silicon layer field of thickness the circuit which used partial depletion mold MOS transistor or this partial depletion mold MOS transistor among the silicon layer fields of two or more kinds of said thickness.
[Claim 6] the semiconductor integrated circuit characterized by having formed in the thin silicon layer field of thickness the circuit which used MOS transistor or this MOS transistor among the silicon layer fields of two or more kinds of said thickness on a semi-conductor substrate according to claim 1, 2, 3, or 4, and forming in the thick silicon layer field of thickness the circuit which used the bipolar transistor or this bipolar transistor among the silicon layer fields of two or more kinds of said thickness.
[Claim 7] The semiconductor integrated circuit characterized by forming a passive component in said silicon layer field on a semi-conductor substrate according to claim 1, 2, 3, or 4.
[Claim 8] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 2, or 4 By making at least 2 times or more of selective oxidation the 1st silicon substrate The process which forms in the front-face side of this 1st silicon substrate the silicon area of exposed oxide where at least three or more kinds of thickness differs, The process which carries out flattening of the front-face side of said 1st silicon substrate, and leaves and removes a part of silicon oxide in said each silicon area of exposed oxide, The manufacture approach of the semi-conductor substrate characterized by performing in order the process which removes lamination ****** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.
[Claim 9] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 3, or 4, while forming a slot in the front-face side of the 1st silicon substrate The process which forms the silicon oxidizing zone from which at least two or more kinds of thickness differs by carrying out at least 1 times or more of selective

oxidation, The process which leaves said some of [at least] silicon oxidation membrane layers, and carries out flattening of the front-face side of said 1st silicon substrate, The manufacture approach of the semi-conductor substrate characterized by performing in order the process which removes lamination ****** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of the semiconductor integrated circuit formed in a semi-conductor substrate and a semi-conductor substrate, and this semi-conductor substrate.
[0002]
[Description of the Prior Art] The CMOS (Complementary Metal Oxide Semiconductor) transistor formed in the semi-conductor substrate, i.e., an SOI (Silicon On Insulattor) substrate, in which the thin film silicon layer was formed on the insulating substrate or the insulator layer has a small junction capacitance between source drains, and by the reason of being able to prevent a latch rise, when advancing low-power-ization of a semiconductor integrated circuit, it attracts attention. In CMOS transistor formed on SOI structure, it is perfect depletion (Fully Depleted). A mold and partial depletion (Partially Depleted) There is a mold. A perfect depletion mold has a thin film silicon layer as thin as about 50nm or less, and the body field inserted into the source field and the drain field is always depletion-ized. In a partial depletion mold, a thin film silicon layer is comparatively as thick as 100nm or more, and the pars basilaris ossis occipitalis of a body field is not depletion-ized. Since perfect depletion mold MOS transistor can make threshold voltage low, a steep subthreshold level property being acquired and controlling OFF leakage current, it is effective in low-power-izing, but since the thin film silicon layer is as thin as about 50nm or less to coincidence, source drain resistance is high, and in order to set up substrate concentration highly, there is a fault of mobility falling and the drive capacity of a transistor declining.
[0003] On the other hand, a subthreshold level property becomes comparable as MOS transistor on a bulk substrate, and partial depletion mold MOS transistor does not have the effectiveness of low-power-izing as large as a perfect depletion mold. However, by fixing the potential of a body field, the hole produced by impact ionization working can be accumulated in a body field, and the phenomenon (kink phenomenon) of making a drain current characteristic producing distortion can be suppressed. Therefore, loading together and semiconductor-integrated-circuit-izing perfect depletion mold MOS transistor and partial depletion mold MOS transistor to the same SOI substrate in consideration of a low-power property and the stability at the time of actuation is proposed.
[0004] Drawing 2 (a) - (e) is the sectional view showing the production process of a semiconductor integrated circuit which used the conventional SOI substrate. When forming MOS transistor of a perfect depletion mold, and MOS transistor of a partial depletion mold in the same SOI substrate conventionally, the process of drawing 2 (a) - (e) is performed in order. First, SIMOX which pours in oxygen ion into a silicon single crystal substrate, and oxidizes in the process of drawing 2 (a) (Separation by IMplanted OXigen) The approach called law, Or by the approach called the lamination method shown in the following reference, the silicon oxidation membrane layer 2 is formed on a silicon substrate 1, and it is about 200nm thin film silicon layer (it is called a "SOI layer" below.) on it. The SOI substrate which has 3 is formed. Reference; JP,5-275663,A [0005] In the process of drawing 2 (b), after forming the buffer layer and silicon

nitride layer of silicon oxide which are not illustrated on a SOI substrate and forming opening in a silicon nitride and silicon oxide through a HOTORISO process, the SOI layer 3 is alternatively oxidized by using this silicon nitride as a mask, and a silicon nitride and silicon oxide are removed. Thereby, a SOI layer forms in 70nm the field 4 which became thin. In the process of drawing 2 (c), the SOI layer 3 is etched alternatively, and while forming the field 6 which forms partial depletion mold MOS transistor in locations other than field 4, the field 5 which forms perfect depletion mold MOS transistor in a location including a field 4 is formed. It is the process of this drawing 2 (c), next CMOS transistor is formed. In addition, although drawing 2 (d) and (e) explain the case where N channel mold MOS transistor (henceforth "NMOS") is formed, also when forming P channel mold MOS transistor (henceforth "PMOS"), it can form at the same process only by replacing the type of an impurity with.
[0006] In the process of drawing 2 (d), the P type impurity for controlling the threshold voltage of MOS transistor is poured in, the laminating of the gate oxide 7 is carried out on the SOI layer 3 of fields 5 and 6, and the polish recon 8 used as a gate electrode is formed on it. Furthermore, it is P+ to the part which injects a high concentration P type impurity into a part of SOI layer 3, and serves as the source of partial depletion mold MOS transistor. A field 9 is generated. N+ which pours an N type impurity into high concentration, and becomes the source and a drain in the process of drawing 2 (e) A field 10 is formed in the SOI layer 3. At this time, it is P+. The part which does not pour in and pour an N type impurity into a part of field 9 is P+. P+ which became as [impurity range] and poured in the N type impurity The pars basilaris ossis occipitalis of a field 9 becomes a P type impurity range. Of the above, perfect depletion mold MOS transistor and partial depletion mold MOS transistor are formed. After carrying out the laminating of the interlayer insulation film to the substrate with which this MOS transistor was formed, opening of the contact hole is carried out to the source, a drain, the gate, and a body contact field, metal wiring is formed, and a semiconductor integrated circuit is manufactured.
[0007]
[Problem(s) to be Solved by the Invention] However, by the manufacture approach which forms a semiconductor integrated circuit, the following technical problems were in the conventional SOI substrate. Since the field 4 which forms the gate electrode of perfect depletion mold MOS transistor had become a concave, in order to form the polish recon 8 used as a gate electrode, when applying the resist film, this resist thickness became thicker than the circumference, and control of a gate length dimension tended to become difficult, and problems, like a gate electrode is narrow in the case of etching were produced, and there were things. Furthermore, since the height of the gate electrode of perfect depletion mold MOS transistor and partial depletion mold MOS transistor differed, it was difficult to double the gate length dimension of both transistors.
[0008]
[Means for Solving the Problem] In order to solve said technical problem, 1st invention is carried out to the following configurations in the SOI substrate which has the silicon layer insulated from the substrate substrate with the dielectric film. That is, said silicon layer forms two or more silicon layer fields with at least two or more kinds of different thickness, and between this each silicon layer field, the front face of each of this silicon layer field is made into the same height while insulating electrically. The 2nd invention has insulated by being filled up with said dielectric between said each silicon layer field in the SOI substrate of the 1st invention. In the SOI substrate of the 1st invention, it dissociates on said dielectric film and the 3rd invention forms said each silicon layer field. In the 1st, the 2nd, or the SOI substrate of the 3rd invention, said each silicon layer field is carrying out 4th invention to the configuration which has the area which can form at least two or more components, respectively.
[0009] Set the 5th invention to a semiconductor integrated circuit, and in the thin silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using perfect depletion mold MOS transistor or this perfect depletion mold MOS transistor is formed. In the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness The circuit using partial depletion mold MOS transistor or this partial depletion mold MOS transistor is formed. Set the 6th invention to a semiconductor integrated circuit, and in the thin silicon layer

field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using MOS transistor or this MOS transistor is formed, and the circuit which used the bipolar transistor or this bipolar transistor is formed in the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness.
[0010] In a semiconductor integrated circuit, the 7th invention can be set on the 1-3rd or the SOI substrate of the 4th invention, and forms the passive component in a silicon layer field. The 8th invention has devised the following approaches in the manufacture approach of a semi-conductor substrate of manufacturing the 1st, 2, or the semi-conductor substrate of the 4th invention. Namely, by making at least 2 times or more of selective oxidation the 1st silicon substrate The process which forms in the front-face side of this 1st silicon substrate at least three or more kinds of silicon area of exposed oxides where thickness differs, The process which carries out flattening of the front-face side of said 1st silicon substrate, and leaves and removes a part of silicon oxide in said each silicon area of exposed oxide, It is made to perform in order the process which removes lamination ****** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.
[0011] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 3, or 4, while the 9th invention forms a slot in the front-face side of the 1st silicon substrate The process which forms at least two or more kinds of silicon oxidizing zones from which thickness differs by carrying out at least 1 times or more of selective oxidation, The process which leaves said some of [at least] silicon oxidation membrane layers, and carries out flattening of the front-face side of said 1st silicon substrate, It is made to perform in order the process which removes lamination ****** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.
[0012] According to the 1st to 9th invention, since the manufacture approach of a SOI substrate, a semiconductor integrated circuit, and a SOI substrate was constituted as mentioned above, the silicon layer field where thickness differs is formed on a dielectric film, and the height of the front face of those silicon layer fields is the same. Therefore, the height of the gate electrode of MOS transistor formed on the silicon field of a SOI substrate will gather. According to the 4th invention, moreover, each silicon layer field Since it has the area which can form at least two or more components, respectively, for example to the thin silicon layer field of thickness A circuit with rapidity and low-power nature and the circuit where stability is searched for are loaded together by the common substrate by forming the circuit using perfect depletion mold MOS transistor, and forming the circuit which used partial depletion mold MOS transistor for the thick silicon layer field of thickness.
[0013]
 [Embodiment of the Invention] The 1st operation gestalt drawing 1 is the sectional view of the SOI substrate in which the 1st operation gestalt of this invention is shown. This SOI substrate has the dielectric film 12 by which the laminating was carried out on the substrate substrate 11 and this substrate substrate 11, and the silicon layer fields 13 and 14 of two kinds of different thickness are formed on this dielectric film 12. between the silicon layer fields 13 and 14 -- a dielectric film 12 -- **** -- while dissociating electrically, the surface height of these silicon layer fields 13 and 14 is the same.
[0014] Drawing 3 (a) - (e) is the sectional view showing the production process of the SOI substrate of drawing 1 . Drawing 4 (a) - (c) is the sectional view showing the production process of a semiconductor integrated circuit which used the SOI substrate of drawing 1 . In order to form the SOI substrate of drawing 1 , the process of drawing 3 (a) - (e) is performed in order. The process of the first drawing 3 (a) is a process which forms the 1st silicon substrate 20 of a three-tiered structure, and after it forms the porosity silicon layer 22 with a thickness of about 20 micrometers in the front face of the P type silicon substrate 21 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 23 of about 200nm thickness by the CVD (Chemical Vapror Deposition) method.
[0015] At the process of next drawing 3 (b) of drawing 3 (a), while carrying out the laminating of

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the silicon oxidation membrane layer 24 used as a buffer layer to the front face of the single-crystal-silicon layer 23, after forming the silicon nitride layer 25, opening of this a part of silicon nitride layer 25 26 is carried out according to a HOTORISO process. And selective oxidation is performed and thickness of the silicon oxide in a part 26 is made into the thickness of about 50nm. In the process of drawing 3 (c), a HOTORISO process is performed to the part 27 of the fields where the silicon nitride layer 25 remains, this silicon nitride layer 25 removes, selective oxidation is performed, and thickness of silicon oxide [in / both / a part 27] which grows up the thickness of the silicon oxide in a part 26 into about 200nm is set to about 150nm.
[0016] After removing the silicon nitride layer 25 which remained in the process of drawing 3 (d), the single-crystal-silicon layer 23 forms the silicon area of exposed oxide 28 which oxidized altogether, the silicon area of exposed oxide 29 which left about 50nm of single-crystal-silicon layers 23, and oxidized, and the silicon area of exposed oxide 30 which left about 100nm of single-crystal-silicon layers 23, and oxidized by performing thermal oxidation.
[0017] In the process of drawing 3 (e), the front face where the substrate of drawing 3 (d) oxidized is evenly ground by a chemical mechanical-polishing method etc. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 31 prepared separately in the substrate with which the front face was ground, and it is ********** firmly. The silicon substrate 31 side of the ******(ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 22 by the side of a substrate 20, and etching removal is carried out. Furthermore, the porosity silicon layer 22 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 23 is not removed by these etching. Therefore, the SOI layers 32 and 33 separated electrically [this substrate 31] in the silicon area of exposed oxides 29 and 30 are formed on a substrate 31. It dissociates electrically between the SOI layers 32 and 33 in the silicon area of exposed oxide 28. That is, the SOI substrate of drawing 1 is formed. A substrate 31 turns into the substrate substrate 11, the silicon area of exposed oxides 28, 29, and 30 serve as a dielectric layer 12, and the SOI layers 32 and 33 serve as the silicon layer fields 13 and 14 where thickness differs.
[0018] In manufacturing the semiconductor integrated circuit which has a CMOS transistor, using the SOI substrate of drawing 1 , it performs the process of drawing 4 (a) - (c) in order. In addition, although drawing 4 (a) - (c) explains the case where NMOS are formed, also when forming PMOS, it can form at the same process only by replacing the type of an impurity with. First, in the process of drawing 4 (a), in order to control the threshold voltage of MOS transistor, after pouring in a P type impurity, carrying out the laminating of the gate oxide 34 to the front face of the SOI layers 32 and 33 which constitute the silicon layer fields 13 and 14, and the exposed dielectric film 12 and applying a resist on this gate oxide 34, a resist pattern is formed by the electron-beam-exposure method. And dry etching which used the resist pattern as the mask is performed, and the gate electrode 35 is formed.
[0019] In the process of drawing 4 (b), silicon oxide is formed all over the main front face, anisotropic etching is performed and a sidewall 36 is formed in the side attachment wall of the gate electrode 35. An N type impurity is poured into the source field and drain field of MOS transistor in the process of drawing 4 (c), and it is N+. After forming a layer 37, the main front face of a substrate is made to carry out selective growth of the W (tungsten) film 38 with a CVD method. Furthermore, after depositing an interlayer insulation film on the main front face of a substrate in which the W film 38 was formed, opening of the contact hole is carried out to the source, a drain, the gate, and a body contact field, and metal wiring is performed. MOS transistor which MOS transistor of a semiconductor integrated circuit was formed of a series of processes of above drawing 4 (a) - (c), and was formed on the thin SOI layer 32 of thickness of them turns into perfect depletion mold MOS transistor, and MOS transistor formed on the thick SOI layer 33 of thickness turns into partial depletion mold MOS transistor. Here, it is formed in a body field without the gate electrode 35 in a space near side of partial depletion mold MOS transistor formed on the thick SOI layer 32 of thickness although the body contact field is not illustrated. That is, it means that perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has contact to a body field had been loaded together by the semiconductor

integrated circuit.
[0020] As mentioned above, while the thick SOI layer 33 of the thickness suitable for forming the thin SOI layer 32 of the thickness which was suitable for forming perfect depletion mold MOS transistor with this 1st operation gestalt with the production process of drawing 3 (a) - (e), and partial depletion mold MOS transistor is separated by the dielectric film 12, the SOI substrate with which that surface height became flat is formed. Therefore, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained. Since perfect depletion mold MOS transistor and partial depletion mold MOS transistor can moreover be formed at the almost same process on the same substrate, while excelling in low cost-ization, productivity improves. Furthermore, since the thickness of the SOI layers 31 and 32 is decided by an epitaxial growth process, an oxidation process, etc. of single crystal silicon, the homogeneity is excellent while control of thickness is easy.
[0021] The 2nd operation gestalt drawing 5 is the sectional view of the SOI substrate in which the 2nd operation gestalt of this invention is shown. This SOI substrate is a substrate which has the silicon layer insulated from the substrate substrate 41 with the dielectric film 42, this silicon layer forms the silicon layer fields 43 and 44 with at least two or more kinds of different thickness, and while insulating electrically between this each silicon layer field 43 and 44 in a slot, the front face of each of these silicon fields 43 and 44 has the same height.
[0022] Drawing 6 (a) - (d) is the sectional view showing the production process of the SOI substrate of drawing 5 , and it explains the manufacture approach of the SOI substrate of drawing 5 , referring to this drawing 6 (a) - (d). First, the process of drawing 6 (a) is a process which forms the 1st silicon substrate 50 of a three-tiered structure, and after it forms the porosity silicon layer 52 with a thickness of about 10 micrometers in the front face of the P type silicon substrate 51 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 53 of about 200nm thickness with a CVD method.
[0023] At the process of next drawing 6 (b) of drawing 6 (a), therefore, silicon oxide 54 is formed in thermal oxidation on the single-crystal-silicon layer 53, and the silicon nitride 55 is further formed on this silicon oxide 54. Then, opening of the silicon nitride 55 and the silicon oxide 54 is carried out partially, according to a HOTORISO process, the single-crystal-silicon layer 53 is etched until it reaches the porosity silicon layer 52, and the structure which divided the single-crystal-silicon layer 53 in the slot 56 is formed. In the process of drawing 6 (c), after a HOTORISO process removes the silicon nitride 55 partially, the silicon area of exposed oxide 57 of about 300nm thickness is formed by selective oxidation.
[0024] In the process of drawing 6 (d), by a chemical mechanical-polishing method etc., it grinds and flattening of the front face is carried out until the silicon nitride 55 is lost. At this time, a part of silicon area of exposed oxide 57 remains, without being ground. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 41 prepared separately in the substrate with which the front face was ground, and it is ********** firmly. The silicon substrate 41 side of the ******(ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 52 by the side of a substrate 50, and etching removal is carried out. Furthermore, the porosity silicon layer 52 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 53 is not removed by these etching. Therefore, the SOI layers 58 and 59 separated electrically [this substrate 41] at silicon oxide 54 and 57 are formed on a substrate 41. Among the SOI layers 58 and 59, there is a slot 56 and it dissociates electrically. That is, the SOI substrate of drawing 5 is formed. Silicon oxide 54 and 57 serves as a dielectric layer 42, and the SOI layers 58 and 59 serve as the silicon layer fields 43 and 44 where thickness differs.
[0025] As mentioned above, while dissociating by the thick SOI layer 59 and thick fang furrow 56 of thickness suitable for forming the thin SOI layer 58 of the thickness which was suitable for

forming perfect depletion mold MOS transistor with this 2nd operation gestalt with drawing 6 (a) - (d), and partial depletion mold MOS transistor, the SOI substrate with which that surface height became flat is formed. Therefore, like the 1st operation gestalt, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained.
[0026] The 3rd operation gestalt drawing 7 is the top view of the SOI substrate in which the 3rd operation gestalt of this invention is shown, and the common sign is given to the element in drawing 1 which shows the 1st operation gestalt, and the common element. It is the substrate manufactured according to the same process as the 1st operation gestalt, and this SOI substrate has the silicon layer field 13 formed in the SOI layer whose thickness is about 50nm, and the silicon layer field 14 formed in the SOI layer whose thickness is about 100nm. It is separated between the silicon layer field 13 and the silicon layer field 14 by the dielectric film 12 formed by the silicon oxidation membrane layer. The silicon layer field 13 and the silicon layer field 14 have the area which can form two or more MOS transistors, respectively, respectively. The digital circuit group which used perfect depletion mold MOS transistor is formed in the thin silicon layer field 13 of thickness, and the analog circuit group which used partial depletion mold MOS transistor is formed in the thick silicon layer field 14 of thickness. By doing in this way, it is possible to load together an analog circuit group and a digital circuit group to a common substrate.
[0027] As mentioned above, with this 3rd operation gestalt, the silicon layer field 13 and the silicon layer field 14 are a SOI substrate with the area which can form two or more MOS transistors, respectively, and mixed loading of an analog circuit group and a digital circuit group is attained. Therefore, an analog circuit group with the high stability at the time of the actuation using the digital circuit group excellent in the rapidity and low-power nature using perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has body contact can be manufactured now to coincidence at the same process. Therefore, the analog digital mixed-loading circuit of high performance can be manufactured by low cost, and productivity is high. Furthermore, since the digital circuit group and the analog circuit group are separated by the dielectric film 12, it can prevent that the noise generated by the digital circuit group arrives at the field of an analog circuit group, and degrades the property of this analog circuit group. If the substrate which formed in the predetermined location beforehand the fields 13 and 14 where the thickness of a SOI layer differs about the product with the respectively almost comparable scale of a digital circuit group and an analog circuit group is moreover created, the period from a circuit design to manufacture can be shortened sharply.
[0028] In addition, this invention is not limited to the above-mentioned operation gestalt, but various deformation is possible for it. As the modification, there is the following, for example.
(1) Although it was made the configuration which forms perfect depletion mold MOS transistor in the thin SOI layers 32 and 58 of thickness, and forms ****** type MOS transistor in the thick SOI layers 33 and 59 of thickness, a bipolar transistor is formed in the thick SOI layers 33 and 59 of this thickness, and you may make it, manufacture the semiconductor integrated circuit consolidated with MOS transistor and a bipolar transistor for example.
(2) In the SOI layers 32, 33, 58, and 59, not only a transistor but passive components, such as in TAKUTA and a capacitor, may be formed and semiconductor-integrated-circuit-ized.
[0029]
[Effect of the Invention] According to the 1st - the 9th invention, as explained to the detail above, the silicon layer field where thickness differs is formed on a dielectric film, and since the height of the front face of those silicon layer fields is the same The height of the gate electrode of MOS transistor formed on this silicon layer field will gather, the die length of this gate electrode can form with a sufficient precision, and formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained. Since perfect depletion mold MOS transistor and partial depletion mold MOS transistor can moreover be formed at the almost

same process on the same substrate, while excelling in low cost-ization, productivity improves.
[0030] Moreover, according to the 4th invention, each silicon layer field Since it has the area which can form at least two or more components, respectively, for example to the thin silicon layer field of thickness A digital circuit with rapidity and low-power nature and the analog circuit where stability is searched for are made in mixed loading at a common substrate by forming the circuit using perfect depletion mold MOS transistor, and forming the circuit which used partial depletion mold MOS transistor for the thick silicon layer field of thickness.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the manufacture approach which forms a semiconductor integrated circuit, the following technical problems were in the conventional SOI substrate. Since the field 4 which forms the gate electrode of perfect depletion mold MOS transistor had become a concave, in order to form the polish recon 8 used as a gate electrode, when applying the resist film, this resist thickness became thicker than the circumference, and control of a gate length dimension tended to become difficult, and problems, like a gate electrode is narrow in the case of etching were produced, and there were things. Furthermore, since the height of the gate electrode of perfect depletion mold MOS transistor and partial depletion mold MOS transistor differed, it was difficult to double the gate length dimension of both transistors.

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
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MEANS

[Means for Solving the Problem] In order to solve said technical problem, 1st invention is carried out to the following configurations in the SOI substrate which has the silicon layer insulated from the substrate substrate with the dielectric film. That is, said silicon layer forms two or more silicon layer fields with at least two or more kinds of different thickness, and between this each silicon layer field, the front face of each of this silicon layer field is made into the same height while insulating electrically. The 2nd invention has insulated by being filled up with said dielectric between said each silicon layer field in the SOI substrate of the 1st invention. In the SOI substrate of the 1st invention, it dissociates on said dielectric film and the 3rd invention forms said each silicon layer field. In the 1st, the 2nd, or the SOI substrate of the 3rd invention, said each silicon layer field is carrying out 4th invention to the configuration which has the area which can form at least two or more components, respectively.
[0009] Set the 5th invention to a semiconductor integrated circuit, and in the thin silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using perfect depletion mold MOS transistor or this perfect depletion mold MOS transistor is formed. In the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness The circuit using partial depletion mold MOS transistor or this partial depletion mold MOS transistor is formed. Set the 6th invention to a semiconductor integrated circuit, and in the thin silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness on the 1-3rd or the SOI substrate of the 4th invention The circuit using MOS transistor or this MOS transistor is formed, and the circuit which used the bipolar transistor or this bipolar transistor is formed in the thick silicon layer field of the thickness of the silicon layer fields of two or more kinds of said thickness.
[0010] In a semiconductor integrated circuit, the 7th invention can be set on the 1-3rd or the SOI substrate of the 4th invention, and forms the passive component in a silicon layer field. The 8th invention has devised the following approaches in the manufacture approach of a semi-conductor substrate of manufacturing the 1st, 2, or the semi-conductor substrate of the 4th invention. Namely, by making at least 2 times or more of selective oxidation the 1st silicon substrate The process which forms in the front-face side of this 1st silicon substrate at least three or more kinds of silicon area of exposed oxides where thickness differs, The process which carries out flattening of the front-face side of said 1st silicon substrate, and leaves and removes a part of silicon oxide in said each silicon area of exposed oxide, It is made to perform in order the process which removes lamination ****** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.
[0011] In the manufacture approach of a semi-conductor substrate of manufacturing a semi-conductor substrate according to claim 1, 3, or 4, while the 9th invention forms a slot in the front-face side of the 1st silicon substrate The process which forms at least two or more kinds of silicon oxidizing zones from which thickness differs by carrying out at least 1 times or more of selective oxidation, The process which leaves said some of [at least] silicon oxidation membrane layers, and carries out flattening of the front-face side of said 1st silicon substrate, It

is made to perform in order the process which removes lamination ****** and said a part of 1st silicon substrate for the 2nd silicon substrate used as said substrate substrate from a rear-face side to the front-face side of said said 1st silicon substrate by which flattening was carried out.
[0012] According to the 1st to 9th invention, since the manufacture approach of a SOI substrate, a semiconductor integrated circuit, and a SOI substrate was constituted as mentioned above, the silicon layer field where thickness differs is formed on a dielectric film, and the height of the front face of those silicon layer fields is the same. Therefore, the height of the gate electrode of MOS transistor formed on the silicon field of a SOI substrate will gather. According to the 4th invention, moreover, each silicon layer field Since it has the area which can form at least two or more components, respectively, for example to the thin silicon layer field of thickness A circuit with rapidity and low-power nature and the circuit where stability is searched for are loaded together by the common substrate by forming the circuit using perfect depletion mold MOS transistor, and forming the circuit which used partial depletion mold MOS transistor for the thick silicon layer field of thickness.
[0013]
[Embodiment of the Invention] The 1st operation gestalt drawing 1 is the sectional view of the SOI substrate in which the 1st operation gestalt of this invention is shown. This SOI substrate has the dielectric film 12 by which the laminating was carried out on the substrate substrate 11 and this substrate substrate 11, and the silicon layer fields 13 and 14 of two kinds of different thickness are formed on this dielectric film 12. between the silicon layer fields 13 and 14 -- a dielectric film 12 -- **** -- while dissociating electrically, the surface height of these silicon layer fields 13 and 14 is the same.
[0014] Drawing 3 (a) - (e) is the sectional view showing the production process of the SOI substrate of drawing 1 . Drawing 4 (a) - (c) is the sectional view showing the production process of a semiconductor integrated circuit which used the SOI substrate of drawing 1 . In order to form the SOI substrate of drawing 1 , the process of drawing 3 (a) - (e) is performed in order. The process of the first drawing 3 (a) is a process which forms the 1st silicon substrate 20 of a three-tiered structure, and after it forms the porosity silicon layer 22 with a thickness of about 20 micrometers in the front face of the P type silicon substrate 21 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 23 of about 200nm thickness by the CVD (Chemical Vapror Deposition) method.
[0015] At the process of next drawing 3 (b) of drawing 3 (a), while carrying out the laminating of the silicon oxidation membrane layer 24 used as a buffer layer to the front face of the single-crystal-silicon layer 23, after forming the silicon nitride layer 25, opening of this a part of silicon nitride layer 25 26 is carried out according to a HOTORISO process. And selective oxidation is performed and thickness of the silicon oxide in a part 26 is made into the thickness of about 50nm. In the process of drawing 3 (c), a HOTORISO process is performed to the part 27 of the fields where the silicon nitride layer 25 remains, this silicon nitride layer 25 removes, selective oxidation is performed, and thickness of silicon oxide [in / both / a part 27] which grows up the thickness of the silicon oxide in a part 26 into about 200nm is set to about 150nm.
[0016] After removing the silicon nitride layer 25 which remained in the process of drawing 3 (d), the single-crystal-silicon layer 23 forms the silicon area of exposed oxide 28 which oxidized altogether, the silicon area of exposed oxide 29 which left about 50nm of single-crystal-silicon layers 23, and oxidized, and the silicon area of exposed oxide 30 which left about 100nm of single-crystal-silicon layers 23, and oxidized by performing thermal oxidation.
[0017] In the process of drawing 3 (e), the front face where the substrate of drawing 3 (d) oxidized is evenly ground by a chemical mechanical-polishing method etc. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 31 prepared separately in the substrate with which the front face was ground, and it is ********** firmly. The silicon substrate 31 side of the ******(ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 22 by the side of a substrate 20, and etching removal is carried out. Furthermore, the porosity silicon layer 22 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 23 is not removed by these etching. Therefore, the SOI layers 32

and 33 separated electrically [this substrate 31] in the silicon area of exposed oxides 29 and 30 are formed on a substrate 31. It dissociates electrically between the SOI layers 32 and 33 in the silicon area of exposed oxide 28. That is, the SOI substrate of drawing 1 is formed. A substrate 31 turns into the substrate substrate 11, the silicon area of exposed oxides 28, 29, and 30 serve as a dielectric layer 12, and the SOI layers 32 and 33 serve as the silicon layer fields 13 and 14 where thickness differs.

[0018] In manufacturing the semiconductor integrated circuit which has a CMOS transistor, using the SOI substrate of drawing 1 , it performs the process of drawing 4 (a) - (c) in order. In addition, although drawing 4 (a) - (c) explains the case where NMOS are formed, also when forming PMOS, it can form at the same process only by replacing the type of an impurity with. First, in the process of drawing 4 (a), in order to control the threshold voltage of MOS transistor, after pouring in a P type impurity, carrying out the laminating of the gate oxide 34 to the front face of the SOI layers 32 and 33 which constitute the silicon layer fields 13 and 14, and the exposed dielectric film 12 and applying a resist on this gate oxide 34, a resist pattern is formed by the electron-beam-exposure method. And dry etching which used the resist pattern as the mask is performed, and the gate electrode 35 is formed.

[0019] In the process of drawing 4 (b), silicon oxide is formed all over the main front face, anisotropic etching is performed and a sidewall 36 is formed in the side attachment wall of the gate electrode 35. An N type impurity is poured into the source field and drain field of MOS transistor in the process of drawing 4 (c), and it is N+. After forming a layer 37, the main front face of a substrate is made to carry out selective growth of the W (tungsten) film 38 with a CVD method. Furthermore, after depositing an interlayer insulation film on the main front face of a substrate in which the W film 38 was formed, opening of the contact hole is carried out to the source, a drain, the gate, and a body contact field, and metal wiring is performed. MOS transistor which MOS transistor of a semiconductor integrated circuit was formed of a series of processes of above drawing 4 (a) - (c), and was formed on the thin SOI layer 32 of thickness of them turns into perfect depletion mold MOS transistor, and MOS transistor formed on the thick SOI layer 33 of thickness turns into partial depletion mold MOS transistor. Here, it is formed in a body field without the gate electrode 35 in a space near side of partial depletion mold MOS transistor formed on the thick SOI layer 32 of thickness although the body contact field is not illustrated. That is, it means that perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has contact to a body field had been loaded together by the semiconductor integrated circuit.

[0020] As mentioned above, while the thick SOI layer 33 of the thickness suitable for forming the thin SOI layer 32 of the thickness which was suitable for forming perfect depletion mold MOS transistor with this 1st operation gestalt with the production process of drawing 3 (a) - (e), and partial depletion mold MOS transistor is separated by the dielectric film 12, the SOI substrate with which that surface height became flat is formed. Therefore, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained. Since perfect depletion mold MOS transistor and partial depletion mold MOS transistor can moreover be formed at the almost same process on the same substrate, while excelling in low cost-ization, productivity improves. Furthermore, since the thickness of the SOI layers 31 and 32 is decided by an epitaxial growth process, an oxidation process, etc. of single crystal silicon, the homogeneity is excellent while control of thickness is easy.

[0021] The 2nd operation gestalt drawing 5 is the sectional view of the SOI substrate in which the 2nd operation gestalt of this invention is shown. This SOI substrate is a substrate which has the silicon layer insulated from the substrate substrate 41 with the dielectric film 42, this silicon layer forms the silicon layer fields 43 and 44 with at least two or more kinds of different thickness, and while insulating electrically between this each silicon layer field 43 and 44 in a slot, the front face of each of these silicon fields 43 and 44 has the same height.

[0022] Drawing 6 (a) - (d) is the sectional view showing the production process of the SOI substrate of drawing 5 , and it explains the manufacture approach of the SOI substrate of drawing 5 , referring to this drawing 6 (a) - (d). First, the process of drawing 6 (a) is a process which forms the 1st silicon substrate 50 of a three-tiered structure, and after it forms the porosity silicon layer 52 with a thickness of about 10 micrometers in the front face of the P type silicon substrate 51 and oxidizes, it carries out EPITAKYARU growth of the single-crystal-silicon layer 53 of about 200nm thickness with a CVD method.
[0023] At the process of next drawing 6 (b) of drawing 6 (a), therefore, silicon oxide 54 is formed in thermal oxidation on the single-crystal-silicon layer 53, and the silicon nitride 55 is further formed on this silicon oxide 54. Then, opening of the silicon nitride 55 and the silicon oxide 54 is carried out partially, according to a HOTORISO process, the single-crystal-silicon layer 53 is etched until it reaches the porosity silicon layer 52, and the structure which divided the single-crystal-silicon layer 53 in the slot 56 is formed. In the process of drawing 6 (c), after a HOTORISO process removes the silicon nitride 55 partially, the silicon area of exposed oxide 57 of about 300nm thickness is formed by selective oxidation.
[0024] In the process of drawing 6 (d), by a chemical mechanical-polishing method etc., it grinds and flattening of the front face is carried out until the silicon nitride 55 is lost. At this time, a part of silicon area of exposed oxide 57 remains, without being ground. Superposition and heat treatment are performed so that this polished surface may touch the 2nd silicon substrate 41 prepared separately in the substrate with which the front face was ground, and it is ********** firmly. The silicon substrate 41 side of the ******(ed) substrate is covered with a silicon nitride, using the mixed liquor of a nitric acid and fluoric acid, it leaves the porosity silicon layer 52 by the side of a substrate 50, and etching removal is carried out. Furthermore, the porosity silicon layer 52 is also removed using the mixed liquor of a nitric acid, fluoric acid, and an acetic acid. The single-crystal-silicon layer 53 is not removed by these etching. Therefore, the SOI layers 58 and 59 separated electrically [this substrate 41] at silicon oxide 54 and 57 are formed on a substrate 41. Among the SOI layers 58 and 59, there is a slot 56 and it dissociates electrically. That is, the SOI substrate of drawing 5 is formed. Silicon oxide 54 and 57 serves as a dielectric layer 42, and the SOI layers 58 and 59 serve as the silicon layer fields 43 and 44 where thickness differs.
[0025] As mentioned above, while dissociating by the thick SOI layer 59 and thick fang furrow 56 of thickness suitable for forming the thin SOI layer 58 of the thickness which was suitable for forming perfect depletion mold MOS transistor with this 2nd operation gestalt with drawing 6 (a) - (d), and partial depletion mold MOS transistor, the SOI substrate with which that surface height became flat is formed. Therefore, like the 1st operation gestalt, if a semiconductor integrated circuit is manufactured using a SOI substrate, a set and the resist thickness to apply become fixed and the height of the polish recon of perfect depletion mold MOS transistor and partial depletion mold MOS transistor can form the die length of the gate electrode 35 in homogeneity with a sufficient precision. Therefore, formation of a good semiconductor integrated circuit without the vena contracta of a pattern etc. is attained.
[0026] The 3rd operation gestalt drawing 7 is the top view of the SOI substrate in which the 3rd operation gestalt of this invention is shown, and the common sign is given to the element in drawing 1 which shows the 1st operation gestalt, and the common element. It is the substrate manufactured according to the same process as the 1st operation gestalt, and this SOI substrate has the silicon layer field 13 formed in the SOI layer whose thickness is about 50nm, and the silicon layer field 14 formed in the SOI layer whose thickness is about 100nm. It is separated between the silicon layer field 13 and the silicon layer field 14 by the dielectric film 12 formed by the silicon oxidation membrane layer. The silicon layer field 13 and the silicon layer field 14 have the area which can form two or more MOS transistors, respectively, respectively. The digital circuit group which used perfect depletion mold MOS transistor is formed in the thin silicon layer field 13 of thickness, and the analog circuit group which used partial depletion mold MOS transistor is formed in the thick silicon layer field 14 of thickness. By doing in this way, it is possible to load together an analog circuit group and a digital circuit group to a common substrate.

[0027] As mentioned above, with this 3rd operation gestalt, the silicon layer field 13 and the silicon layer field 14 are a SOI substrate with the area which can form two or more MOS transistors, respectively, and mixed loading of an analog circuit group and a digital circuit group is attained. Therefore, an analog circuit group with the high stability at the time of the actuation using the digital circuit group excellent in the rapidity and low-power nature using perfect depletion mold MOS transistor and partial depletion mold MOS transistor which has body contact can be manufactured now to coincidence at the same process. Therefore, the analog digital mixed-loading circuit of high performance can be manufactured by low cost, and productivity is high. Furthermore, since the digital circuit group and the analog circuit group are separated by the dielectric film 12, it can prevent that the noise generated by the digital circuit group arrives at the field of an analog circuit group, and degrades the property of this analog circuit group. If the substrate which formed in the predetermined location beforehand the fields 13 and 14 where the thickness of a SOI layer differs about the product with the respectively almost comparable scale of a digital circuit group and an analog circuit group is moreover created, the period from a circuit design to manufacture can be shortened sharply.
[0028] In addition, this invention is not limited to the above-mentioned operation gestalt, but various deformation is possible for it. As the modification, there is the following, for example.
(1) Although it was made the configuration which forms perfect depletion mold MOS transistor in the thin SOI layers 32 and 58 of thickness, and forms ****** type MOS transistor in the thick SOI layers 33 and 59 of thickness, a bipolar transistor is formed in the thick SOI layers 33 and 59 of this thickness, and you may make it, manufacture the semiconductor integrated circuit consolidated with MOS transistor and a bipolar transistor for example.
(2) In the SOI layers 32, 33, 58, and 59, not only a transistor but passive components, such as in TAKUTA and a capacitor, may be formed and semiconductor-integrated-circuit-ized.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the SOI substrate in which the 1st operation gestalt of this invention is shown.
[Drawing 2] It is the sectional view showing the production process of the semiconductor integrated circuit using the conventional SOI substrate.
[Drawing 3] It is the sectional view showing the production process of the SOI substrate of drawing 1 .
[Drawing 4] It is the sectional view showing the production process of the semiconductor integrated circuit using the SOI substrate of drawing 1 .
[Drawing 5] It is the sectional view of the SOI substrate in which the 2nd operation gestalt of this invention is shown.
[Drawing 6] It is the sectional view showing the production process of the SOI substrate of drawing 5 .
[Drawing 7] It is the top view of the SOI substrate in which the 3rd operation gestalt of this invention is shown.
[Description of Notations]
11 41 Substrate substrate
12 42 Dielectric film
32, 33, 43, 44 Silicon layer field
20 50 The 1st silicon substrate

[Translation done.]

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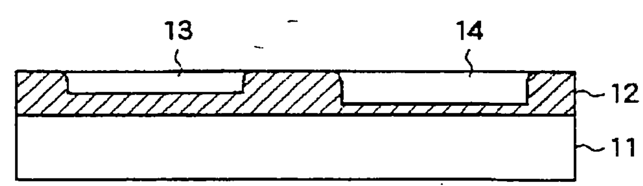
(54)【発明の名称】　半導体基板、半導体集積回路及び半導体基板の製造方法

(57)【要約】
【課題】　ＳＯＩ基板において、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタのゲートを精度よく形成する。
【解決手段】　ＳＯＩ基板は、下地基板１１と、下地基板１１上に積層された誘電体膜１２とを有しているが、該誘電体膜１２の上には異なる２種類の膜厚のシリコン層領域１３、１４が形成されている。シリコン層領域１３，１４の表面高さは同じになっている。そのため、シリコン層領域１３，１４上に形成されるトランジスタのゲート電極の高さを揃えることができ、塗布するレジスト厚さが均一化でき、ゲート長を精度よく形成できる。

11：下地基板
12：誘電体膜
13, 14：シリコン層領域



本発明の第１の実施形態の SOI 基板

【特許請求の範囲】

【請求項１】　誘電体膜によって下地基板から絶縁されたシリコン層を有する半導体基板において、
前記シリコン層は異なる少なくとも２種類以上の膜厚を持つ複数のシリコン層領域を形成し、該各シリコン層領域間は電気的に絶縁すると共に該各シリコン層領域の表面は同じ高さにしたことを特徴とする半導体基板。

【請求項２】　前記各シリコン層領域間は、前記誘電体を充填することで絶縁したことを特徴とする請求項１記載の半導体基板。

【請求項３】　前記各シリコン層領域は、前記誘電体膜上に分離して形成したことを特徴とする請求項１記載の半導体基板。

【請求項４】　前記各シリコン層領域は、少なくとも２個以上の素子が形成可能な面積をそれぞれ有することを特徴とする請求項１、２または３記載の半導体基板。

【請求項５】　請求項１、２、３または４記載の半導体基板上における前記２種類以上の膜厚のシリコン層領域のうち、膜厚の薄いシリコン層領域には完全空乏型ＭＯＳトランジスタまたは該完全空乏型ＭＯＳトランジスタを用いた回路を形成し、
前記２種類以上の膜厚のシリコン層領域のうち、膜厚の厚いシリコン層領域には部分空乏型ＭＯＳトランジスタまたは該部分空乏型ＭＯＳトランジスタを用いた回路を形成したことを特徴とする半導体集積回路。

【請求項６】　請求項１、２、３または４記載の半導体基板上における前記２種類以上の膜厚のシリコン層領域のうち、膜厚の薄いシリコン層領域にはＭＯＳトランジスタまたは該ＭＯＳトランジスタを用いた回路を形成し、
前記２種類以上の膜厚のシリコン層領域のうち、膜厚の厚いシリコン層領域にはバイポーラトランジスタまたは該バイポーラトランジスタを用いた回路を形成したことを特徴とする半導体集積回路。

【請求項７】　請求項１、２、３または４記載の半導体基板上における前記シリコン層領域には、パッシブ素子を形成したことを特徴とする半導体集積回路。

【請求項８】　請求項１、２または４記載の半導体基板を製造する半導体基板の製造方法において、
第１のシリコン基板に少なくとも２回以上の選択酸化をすることにより、少なくとも３種類以上の膜厚の異なるシリコン酸化膜領域を該第１のシリコン基板の表面側に形成する工程と、
前記第１のシリコン基板の表面側を平坦化し、前記各シリコン酸化膜領域におけるシリコン酸化膜の一部を残して除去する工程と、
前記平坦化された前記第１のシリコン基板の表面側に前記下地基板となる第２のシリコン基板を貼合わせる工程と、
前記第１のシリコン基板の一部を裏面側から除去する工程とを、順に行うことを特徴とする半導体基板の製造方法。

【請求項９】　請求項１、３または４記載の半導体基板を製造する半導体基板の製造方法において、
第１のシリコン基板の表面側に溝を形成すると共に、少なくとも１回以上の選択酸化をすることにより、少なくとも２種類以上の膜厚の異なるシリコン酸化層を形成する工程と、
前記第１のシリコン基板の表面側を少なくとも一部の前記シリコン酸化膜層を残して平坦化する工程と、
前記平坦化された前記第１のシリコン基板の表面側に前記下地基板となる第２のシリコン基板を貼合わせる工程と、
前記第１のシリコン基板の一部を裏面側から除去する工程とを、順に行うことを特徴とする半導体基板の製造方法。

【発明の詳細な説明】

【０００１】
【産業上の利用分野】本発明は、半導体基板、半導体基板に形成される半導体集積回路及び該半導体基板の製造方法に関するものである。

【０００２】
【従来の技術】絶縁基板または絶縁膜上に薄膜シリコン層を形成した半導体基板、つまり、ＳＯＩ（Silicon On Insulattor)基板に形成されたＣＭＯＳ（Complementary Metal Oxide Semiconductor)トランジスタは、ソース・ドレイン間の接合容量が小さく、ラッチアップを防止できる等の理由で、半導体集積回路の低消費電力化を進める上で、注目されている。ＳＯＩ構造上に形成されるＣＭＯＳトランジスタには、完全空乏（Fully Depleted）型と部分空乏（Partially Depleted）型とがある。完全空乏型は、薄膜シリコン層が５０ｎｍ程度以下と薄く、ソース領域及びドレイン領域に挟まれたボディ領域が常に空乏化されている。部分空乏型では、薄膜シリコン層が１００ｎｍ以上と比較的厚く、ボディ領域の底部が空乏化されていない。完全空乏型ＭＯＳトランジスタは、急峻なサブスレッショルド特性が得られ、オフリーク電流を抑制しつつ閾値電圧を低くできるので、低消費電力化に有効であるが、同時に薄膜シリコン層が５０ｎｍ程度以下と薄いので、ソース・ドレイン抵抗が高く、基板濃度を高く設定するために易動度が低下してトランジスタの駆動能力が低下する等の欠点がある。

【０００３】これに対し、部分空乏型ＭＯＳトランジスタは、サブスレッショルド特性がバルク基板上のＭＯＳトランジスタと同程度となり、低消費電力化の効果が完全空乏型程には大きくない。しかしながら、ボディ領域の電位を固定することにより、動作中にインパクトイオン化によって生じた空孔がボディ領域に蓄積し、ドレイン電流特性に歪みを生じさせる現象（キンク現象）を抑えることができる。よって、低消費電力特性と動作時の

安定性とを考慮し、同一ＳＯＩ基板に完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタとを混載して半導体集積回路化することが提案されている。

【０００４】図２（ａ）～（ｅ）は、従来のＳＯＩ基板を用いた半導体集積回路の製造工程を示す断面図である。従来、同一ＳＯＩ基板に完全空乏型のＭＯＳトランジスタと部分空乏型のＭＯＳトランジスタとを形成するときには、図２（ａ）～（ｅ）の工程を順に行う。まず、図２（ａ）の工程において、シリコン単結晶基板中に酸素イオンを注入して酸化するＳＩＭＯＸ（Separation by IMplanted OXigen）法と呼ばれる方法、あるいは次の文献に示される貼合わせ法と呼ばれる方法により、シリコン基板１上にシリコン酸化膜層２を形成し、その上に約２００ｎｍ程度の薄膜シリコン層（以下「ＳＯＩ層」という。）３を有するＳＯＩ基板を形成する。文献；特開平５－２７５６６３号公報

【０００５】図２（ｂ）の工程において、ＳＯＩ基板上に図示しないシリコン酸化膜のバッファ層及びシリコン窒化膜層を形成し、ホトリソ工程を経てシリコン窒化膜及びシリコン酸化膜に開口部を形成した後、該シリコン窒化膜をマスクとしてＳＯＩ層３を選択的に酸化し、シリコン窒化膜及びシリコン酸化膜を除去する。これにより、ＳＯＩ層が例えば７０ｎｍに薄くなった領域４を形成する。図２（ｃ）の工程において、ＳＯＩ層３を選択的にエッチングし、領域４以外の場所に、部分空乏型ＭＯＳトランジスタを形成する領域６を形成すると共に、領域４を含む場所に完全空乏型ＭＯＳトランジスタを形成する領域５を形成する。この図２（ｃ）の工程の次に、ＣＭＯＳトランジスタを形成する。なお、図２（ｄ）及び（ｅ）では、Ｎチャネル型ＭＯＳトランジスタ（以下「ＮＭＯＳ」という。）を形成する場合を説明しているが、Ｐチャネル型ＭＯＳトランジスタ（以下「ＰＭＯＳ」という）を形成する場合も、不純物のタイプを代えるだけで同様の工程で形成できる。

【０００６】図２（ｄ）の工程において、ＭＯＳトランジスタの閾値電圧を制御するためのＰ型不純物を注入し、ゲート酸化膜７を領域５，６のＳＯＩ層３上に積層し、その上にゲート電極となるポリシリコン８を形成する。さらに、ＳＯＩ層３の一部に高濃度Ｐ型不純物を注入し、部分空乏型ＭＯＳトランジスタのソースとなる部分にP^+領域９を生成する。図２（ｅ）の工程において、Ｎ型不純物を高濃度に注入し、ソース及びドレインとなるN^+領域１０をＳＯＩ層３に形成する。このとき、P^+領域９の一部には、Ｎ型不純物を注入せず、注入しない部分はP^+不純物領域のままとなり、Ｎ型不純物を注入したP^+領域９の底部は、Ｐ型不純物領域になる。以上により、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタとが形成される。このＭＯＳトランジスタが形成された基板に層間絶縁膜を積層した後、ソース、ドレイン、ゲート及びボディコンタクト領域にコンタクトホールを開口し、メタル配線を形成して半導体集積回路を製造する。

【０００７】

【発明が解決しようとする課題】しかしながら、従来のＳＯＩ基板に半導体集積回路を形成する製造方法では、次のような課題があった。完全空乏型ＭＯＳトランジスタのゲート電極を形成する領域４が、凹状になっているので、ゲート電極となるポリシリコン８を形成するためにレジスト膜を塗布する際に、該レジスト膜厚が周辺より厚くなり、ゲート長寸法の制御が困難になりやすく、また、エッチングの際にゲート電極がくびれる等の問題を生じことがあった。さらに、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタのゲート電極の高さが異なるので、両方のトランジスタのゲート長寸法を合わせることが困難であった。

【０００８】

【課題を解決するための手段】前記課題を解決するために、第１の発明は、誘電体膜によって下地基板から絶縁されたシリコン層を有するＳＯＩ基板において、次のような構成にしている。即ち、前記シリコン層は異なる少なくとも２種類以上の膜厚を持つ複数のシリコン層領域を形成し、該各シリコン層領域間は電気的に絶縁すると共に該各シリコン層領域の表面は同じ高さにしている。第２の発明は、第１の発明のＳＯＩ基板において、前記各シリコン層領域の間は、前記誘電体を充填することで絶縁している。第３の発明は、第１の発明のＳＯＩ基板において、前記各シリコン層領域は、前記誘電体膜上に分離されて形成している。第４の発明は、第１、第２または第３の発明のＳＯＩ基板において、前記各シリコン層領域は、少なくとも２個以上の素子が形成可能な面積をそれぞれ有する構成にしている。

【０００９】第５の発明は、半導体集積回路において、第１～３または第４の発明のＳＯＩ基板上における前記２種類以上の膜厚のシリコン層領域のうちの膜厚の薄いシリコン層領域には、完全空乏型ＭＯＳトランジスタまたは該完全空乏型ＭＯＳトランジスタを用いた回路を形成し、前記２種類以上の膜厚のシリコン層領域のうちの膜厚の厚いシリコン層領域には、部分空乏型ＭＯＳトランジスタまたは該部分空乏型ＭＯＳトランジスタを用いた回路を形成している。第６の発明は、半導体集積回路において、第１～３または第４の発明のＳＯＩ基板上における前記２種類以上の膜厚のシリコン層領域のうちの膜厚の薄いシリコン層領域には、ＭＯＳトランジスタまたは該ＭＯＳトランジスタを用いた回路を形成し、前記２種類以上の膜厚のシリコン層領域のうちの膜厚の厚いシリコン層領域には、バイポーラトランジスタまたは該バイポーラトランジスタを用いた回路を形成している。

【００１０】第７の発明は、半導体集積回路において、第１～３または第４の発明のＳＯＩ基板上におけシリコン層領域には、パッシブ素子を形成している。第８の発

明は、第１、２または第４の発明の半導体基板を製造する半導体基板の製造方法において、次のような方法を講じている。即ち、第１のシリコン基板に少なくとも２回以上の選択酸化をすることにより、膜厚の異なる少なくとも３種類以上のシリコン酸化膜領域を該第１のシリコン基板の表面側に形成する工程と、前記第１のシリコン基板の表面側を平坦化し、前記各シリコン酸化膜領域におけるシリコン酸化膜の一部を残して除去する工程と、前記平坦化された前記第１のシリコン基板の表面側に前記下地基板となる第２のシリコン基板を貼合わせる工程と、前記第１のシリコン基板の一部を裏面側から除去する工程とを、順に行うようにしている。

【００１１】第９の発明は、請求項１、３または４記載の半導体基板を製造する半導体基板の製造方法において、第１のシリコン基板の表面側に溝を形成すると共に、少なくとも１回以上の選択酸化をすることにより、膜厚の異なる少なくとも２種類以上のシリコン酸化層を形成する工程と、前記第１のシリコン基板の表面側を少なくとも一部の前記シリコン酸化膜層を残して平坦化する工程と、前記平坦化された前記第１のシリコン基板の表面側に前記下地基板となる第２のシリコン基板を貼合わせる工程と、前記第１のシリコン基板の一部を裏面側から除去する工程とを、順に行うようにしている。

【００１２】第１から第９の発明によれば、以上のようにＳＯＩ基板、半導体集積回路及びＳＯＩ基板の製造方法を構成したので、膜厚の異なるシリコン層領域が誘電体膜上に形成され、かつ、それらのシリコン層領域の表面の高さが同じである。そのため、ＳＯＩ基板のシリコン領域上に形成するＭＯＳトランジスタのゲート電極の高さが揃うことになる。また、第４の発明によれば、各シリコン層領域は、少なくとも２個以上の素子が形成可能な面積をそれぞれ持つので、例えば膜厚の薄いシリコン層領域に、完全空乏型ＭＯＳトランジスタを用いた回路を形成し、膜厚の厚いシリコン層領域に、部分空乏型ＭＯＳトランジスタを用いた回路を形成することで、高速性及び低消費電力性を持つ回路と、安定性が求められる回路とが共通基板に混載される。

【００１３】

【発明の実施の形態】第１の実施形態

図１は、本発明の第１の実施形態を示すＳＯＩ基板の断面図である。このＳＯＩ基板は、下地基板１１と、該下地基板１１上に積層された誘電体膜１２とを有し、該誘電体膜１２の上には異なる２種類の膜厚のシリコン層領域１３、１４が形成されている。シリコン層領域１３，１４の間は、誘電体膜１２にって電気的に分離されると共に、該シリコン層領域１３、１４の表面高さは、同じになっている。

【００１４】図３（ａ）～（ｅ）は、図１のＳＯＩ基板の製造工程を示す断面図である。図４（ａ）～（ｃ）は、図１のＳＯＩ基板を用いた半導体集積回路の製造工程を示す断面図である。図１のＳＯＩ基板を形成するには、図３（ａ）～（ｅ）の工程を順に行う。最初の図３（ａ）の工程は、３層構造の第１のシリコン基板２０を形成する工程であり、Ｐ型シリコン基板２１の表面に約２０μｍの厚さの多孔質シリコン層２２を形成して酸化した後、ＣＶＤ（Chemical Vapror Deposition）法により、約２００ｎｍ厚の単結晶シリコン層２３をエピタキャル成長させる。

【００１５】図３（ａ）の次の図３（ｂ）の工程では、単結晶シリコン層２３の表面にバッファ層となるシリコン酸化膜層２４を積層すると共にシリコン窒化膜層２５を形成した後、ホトリソ工程により該シリコン窒化膜層２５の一部分２６を開口する。そして、選択酸化を行い、部分２６におけるシリコン酸化膜の膜厚を約５０ｎｍの厚さにする。図３（ｃ）の工程において、シリコン窒化膜層２５が残っている領域のうちの一部分２７に対してホトリソ工程を行い該シリコン窒化膜層２５の除去し、選択酸化を行い、部分２６におけるシリコン酸化膜の膜厚を約２００ｎｍに成長させる共に、部分２７におけるシリコン酸化膜の膜厚を例えば約１５０ｎｍにする。

【００１６】図３（ｄ）の工程において、残ったシリコン窒化膜層２５を除去した後、熱酸化を行うことにより、単結晶シリコン層２３がすべて酸化されたシリコン酸化膜領域２８と、単結晶シリコン層２３を約５０ｎｍ残して酸化されたシリコン酸化膜領域２９と、単結晶シリコン層２３を約１００ｎｍ残して酸化されたシリコン酸化膜領域３０とを形成する。

【００１７】図３（ｅ）の工程において、化学的機械研磨法等により、図３（ｄ）の基板の酸化された表面を平坦に研磨する。表面が研磨された基板を、別途用意された第２のシリコン基板３１に、該研磨面が接するように重ね合せ、熱処理を行って強固に貼合わせる。貼合わされた基板のシリコン基板３１側をシリコン窒化膜で被覆し、硝酸とフッ酸の混合液を用いて基板２０側の多孔質シリコン層２２を残してエッチング除去する。さらに、硝酸とフッ酸と酢酸の混合液を用いてその多孔質シリコン層２２も除去する。これらのエッチングでは、単結晶シリコン層２３は除去されない。よって、基板３１の上に、該基板３１とはシリコン酸化膜領域２９，３０で電気的に分離されたＳＯＩ層３２，３３が形成される。ＳＯＩ層３２，３３の間は、シリコン酸化膜領域２８で電気的に分離されている。即ち、図１のＳＯＩ基板が形成されている。基板３１が下地基板１１となり、シリコン酸化膜領域２８，２９，３０が誘電体層１２となり、ＳＯＩ層３２，３３が、膜厚が異なるシリコン層領域１３，１４となる。

【００１８】図１のＳＯＩ基板を用いて例えばＣＭＯＳトランジスタを持つ半導体集積回路を製造する場合には、図４（ａ）～（ｃ）の工程を順に行う。なお、図４

（ａ）～（ｃ）では、ＮＭＯＳを形成する場合を説明しているが、ＰＭＯＳを形成する場合も、不純物のタイプを代えるだけで同様の工程で形成できる。まず、図４（ａ）の工程において、ＭＯＳトランジスタの閾値電圧を制御するためにＰ型不純物を注入し、シリコン層領域１３，１４を構成するＳＯＩ層３２，３３及び露出した誘電体膜１２の表面にゲート酸化膜３４を積層し、該ゲート酸化膜３４上にレジストを塗布した後、電子ビーム露光法によってレジストパタンを形成する。そして、レジストパタンをマスクとしたドライエッチングを行い、ゲート電極３５を形成する。

【００１９】図４（ｂ）の工程において、主表面全面にシリコン酸化膜を形成し、異方性エッチングを行い、ゲート電極３５の側壁にサイドウォール３６を形成する。図４（ｃ）の工程において、ＭＯＳトランジスタのソース領域とドレイン領域とに、Ｎ型不純物を注入してN^+層３７を形成した後、ＣＶＤ法により、Ｗ（タングステン）膜３８を基板の主表面に選択成長させる。さらに、Ｗ膜３８が形成された基板の主表面に層間絶縁膜を堆積した後、ソース、ドレイン、ゲート及びボディコンタクト領域にコンタクトホールを開口して、メタル配線を行う。以上の図４（ａ）～（ｃ）の一連の工程により、半導体集積回路のＭＯＳトランジスタが形成され、膜厚の薄いＳＯＩ層３２の上に形成されたＭＯＳトランジスタが完全空乏型ＭＯＳトランジスタとなり、膜厚の厚いＳＯＩ層３３の上に形成されたＭＯＳトランジスタが部分空乏型ＭＯＳトランジスタになる。ここで、ボディコンタクト領域は図示していないが、膜厚の厚いＳＯＩ層３２上に形成される部分空乏型ＭＯＳトランジスタの例えば紙面手前側にある、ゲート電極３５のないボディ領域に形成される。つまり、完全空乏型ＭＯＳトランジスタと、ボディ領域にコンタクトを有する部分空乏型ＭＯＳトランジスタとが半導体集積回路に混載されたことになる。

【００２０】以上のように、この第１の実施形態では、図３（ａ）～（ｅ）の製造工程で、完全空乏型ＭＯＳトランジスタを形成するのに適した膜厚の薄いＳＯＩ層３２と部分空乏型ＭＯＳトランジスタを形成するのに適した膜厚の厚いＳＯＩ層３３とが誘電体膜１２で分離されると共にその表面高さが平坦になったＳＯＩ基板を形成している。そのため、ＳＯＩ基板を用いて半導体集積回路を製造すると、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタのポリシリコンの高さが揃い、塗布するレジスト膜厚が一定となり、ゲート電極３５の長さを精度良く均一に形成できる。よって、パタンのくびれ等のない良好な半導体集積回路の形成が可能になる。その上、同一基板上に、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタとをほぼ同一の工程で形成できるので、低コスト化に優れると共に、生産性が向上する。さらに、ＳＯＩ層３１，３２の膜厚が、単結晶シリコンのエピタキシャル成長工程及び酸化工程等で決まるので、膜厚の制御が容易であると共にその均一性が優れている。

【００２１】<u>第２の実施形態</u>
図５は、本発明の第２の実施形態を示すＳＯＩ基板の断面図である。このＳＯＩ基板は、下地基板４１から誘電体膜４２によって絶縁されたシリコン層を有する基板であって、該シリコン層は異なる少なくとも２種類以上の膜厚を持つシリコン層領域４３，４４を形成し、該各シリコン層領域４３，４４間は溝で電気的に絶縁されると共に該各シリコン領域４３，４４の表面は同じ高さになっている。

【００２２】図６（ａ）～（ｄ）は、図５のＳＯＩ基板の製造工程を示す断面図であり、この図６（ａ）～（ｄ）を参照しつつ、図５のＳＯＩ基板の製造方法を説明する。まず、図６（ａ）の工程は、３層構造の第１のシリコン基板５０を形成する工程であり、Ｐ型シリコン基板５１の表面に約１０μｍの厚さの多孔質シリコン層５２を形成して酸化した後、ＣＶＤ法により、約２００ｎｍ厚の単結晶シリコン層５３をエピタキャル成長させる。

【００２３】図６（ａ）の次の図６（ｂ）の工程では、熱酸化によつて単結晶シリコン層５３上にシリコン酸化膜５４を形成し、さらに、該シリコン酸化膜５４上にシリコン窒化膜５５を形成する。続いて、ホトリソ工程により、シリコン窒化膜５５及びシリコン酸化膜５４を部分的に開口し、単結晶シリコン層５３を多孔質シリコン層５２に届くまでエッチングし、単結晶シリコン層５３を溝５６で分断した構造を形成する。図６（ｃ）の工程において、ホトリソ工程によってシリコン窒化膜５５を部分的に除去した後、選択酸化により、約３００ｎｍ厚のシリコン酸化膜領域５７を形成する。

【００２４】図６（ｄ）の工程において、化学的機械研磨法等により、シリコン窒化膜５５がなくなるまで、研磨して表面を平坦化する。このとき、シリコン酸化膜領域５７の一部は研磨されずに残る。表面が研磨された基板を、別途用意された第２のシリコン基板４１に、該研磨面が接するように重ね合せ、熱処理を行って強固に貼合わせる。貼合わされた基板のシリコン基板４１側をシリコン窒化膜で被覆し、硝酸とフッ酸の混合液を用いて基板５０側の多孔質シリコン層５２を残してエッチング除去する。さらに、硝酸とフッ酸と酢酸の混合液を用いてその多孔質シリコン層５２も除去する。これらのエッチングでは、単結晶シリコン層５３は除去されない。よって、基板４１の上に、該基板４１とはシリコン酸化膜５４，５７で電気的に分離されたＳＯＩ層５８，５９が形成される。ＳＯＩ層５８，５９の間には、溝５６があり、電気的に分離されている。即ち、図５のＳＯＩ基板が形成されている。シリコン酸化膜５４，５７が誘電体層４２となり、ＳＯＩ層５８，５９が、膜厚が異なるシ

リコン層領域４３，４４となる。

【００２５】以上のように、この第２の実施形態では、図６（ａ）～（ｄ）で、完全空乏型ＭＯＳトランジスタを形成するのに適した膜厚の薄いＳＯＩ層５８と部分空乏型ＭＯＳトランジスタを形成するのに適した膜厚の厚いＳＯＩ層５９とが溝５６で分離されると共にその表面高さが平坦になったＳＯＩ基板を形成している。そのため、第１の実施形態と同様に、ＳＯＩ基板を用いて半導体集積回路を製造すると、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタのポリシリコンの高さが揃い、塗布するレジスト膜厚が一定となり、ゲート電極３５の長さを精度良く均一に形成できる。よって、パタンのくびれ等のない良好な半導体集積回路の形成が可能になる。

【００２６】第３の実施形態

図７は、本発明の第３の実施形態を示すＳＯＩ基板の平面図であり、第１の実施形態を示す図１中の要素と共通の要素には共通の符号が付されている。このＳＯＩ基板は、例えば第１の実施形態と同様の工程によって製造された基板であり、膜厚が約５０ｎｍのＳＯＩ層で形成されたシリコン層領域１３と、膜厚が約１００ｎｍのＳＯＩ層で形成されたシリコン層領域１４とを有している。シリコン層領域１３とシリコン層領域１４との間は、シリコン酸化膜層で形成された誘電体膜１２で分離されている。シリコン層領域１３及びシリコン層領域１４は、それぞれ２個以上のＭＯＳトランジスタが形成可能な面積をそれぞれ持っている。膜厚の薄いシリコン層領域１３には、完全空乏型ＭＯＳトランジスタを用いたディジタル回路群を形成し、膜厚の厚いシリコン層領域１４には、部分空乏型ＭＯＳトランジスタを用いたアナログ回路群を形成するようになっている。このようにすることで、アナログ回路群とディジタル回路群とを共通の基板に混載することが可能になっている。

【００２７】以上のように、この第３の実施形態では、シリコン層領域１３及びシリコン層領域１４が、それぞれ２個以上のＭＯＳトランジスタが形成可能な面積を持つＳＯＩ基板になっており、アナログ回路群とディジタル回路群とが混載可能になっている。そのため、完全空乏型ＭＯＳトランジスタを用いた、高速性及び低消費電力性に優れたディジタル回路群と、ボディコンタクトを有する部分空乏型ＭＯＳトランジスタを用いた、動作時の安定性が高いアナログ回路群とを、同様の工程で同時に製造できるようになる。よって、高性能のアナログ・ディジタル混載回路を低コストで製造でき、生産性が高い。さらに、ディジタル回路群とアナログ回路群とが誘電体膜１２で分離されているため、ディジタル回路群で発生する雑音が、アナログ回路群の領域に到達して該アナログ回路群の特性を劣化させることが防止できる。その上、ディジタル回路群とアナログ回路群の規模がそれぞれほぼ同程度の製品について、予め、ＳＯＩ層の膜厚が異なる領域１３，１４を所定の場所に形成した基板を作成しておけば、回路設計から製造までの期間が大幅に短縮できる。

【００２８】なお、本発明は、上記実施形態に限定されず種々の変形が可能である。その変形例としては、例えば次のようなものがある。

（１）　膜厚の薄いＳＯＩ層３２，５８に完全空乏型ＭＯＳトランジスタを形成し、膜厚の厚いＳＯＩ層３３，５９に部分空乏型ＭＯＳトランジスタを形成する構成にしたが、例えば、バイポーラトランジスタを該膜厚の厚いＳＯＩ層３３，５９に形成し、ＭＯＳトランジスタとバイポーラトランジスタとを混載した半導体集積回路を製造するようにしてもよい。

（２）　ＳＯＩ層３２，３３，５８，５９には、トランジスタばかりでなく、インタクタやキャパシタ等のパッシブ素子も形成して半導体集積回路化してもよい。

【００２９】

【発明の効果】以上詳細に説明したように、第１～第９の発明によれば、膜厚の異なるシリコン層領域が誘電体膜上に形成され、かつ、それらのシリコン層領域の表面の高さが同じであるので、該シリコン層領域上に形成されるＭＯＳトランジスタのゲート電極の高さが揃うことになり、該ゲート電極の長さが精度よく形成でき、パタンのくびれ等のない良好な半導体集積回路の形成が可能になる。その上、同一基板上に、完全空乏型ＭＯＳトランジスタと部分空乏型ＭＯＳトランジスタとをほぼ同一の工程で形成できるので、低コスト化に優れると共に、生産性が向上する。

【００３０】そのうえ、第４の発明によれば、各シリコン層領域は、少なくとも２個以上の素子が形成可能な面積をそれぞれ持つので、例えば膜厚の薄いシリコン層領域に、完全空乏型ＭＯＳトランジスタを用いた回路を形成し、膜厚の厚いシリコン層領域に、部分空乏型ＭＯＳトランジスタを用いた回路を形成することで、高速性及び低消費電力性を持つディジタル回路と、安定性が求められるアナログ回路とが共通基板に混載にできる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態を示すＳＯＩ基板の断面図である。

【図２】従来のＳＯＩ基板を用いた半導体集積回路の製造工程を示す断面図である。

【図３】図１のＳＯＩ基板の製造工程を示す断面図である。

【図４】図１のＳＯＩ基板を用いた半導体集積回路の製造工程を示す断面図である。

【図５】本発明の第２の実施形態を示すＳＯＩ基板の断面図である。

【図６】図５のＳＯＩ基板の製造工程を示す断面図である。

【図７】本発明の第３の実施形態を示すＳＯＩ基板の平

面図である。

【符号の説明】

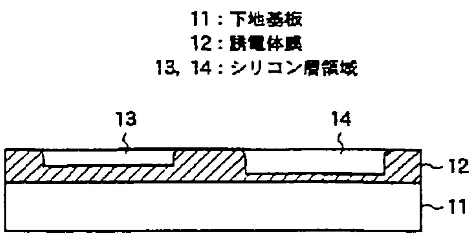
１１，４１　下地基板

１２，４２　誘電体膜

３２，３３，４３，４４　シリコン層領域

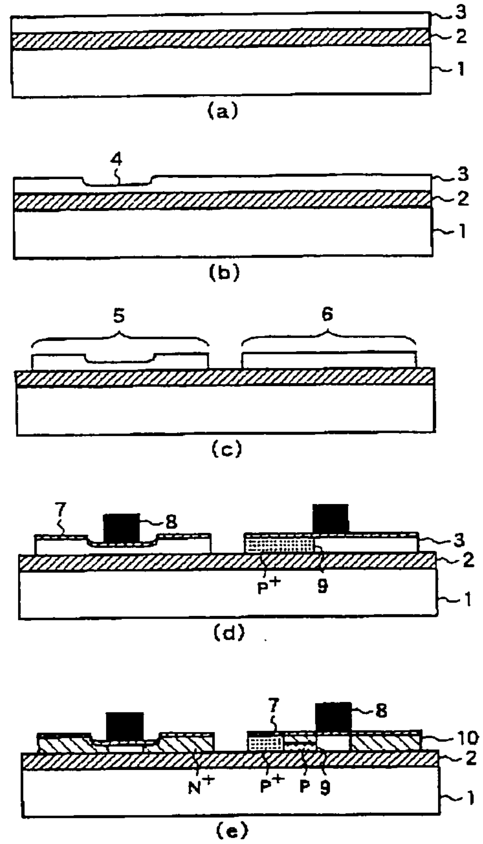
２０，５０　第１のシリコン基板

【図１】



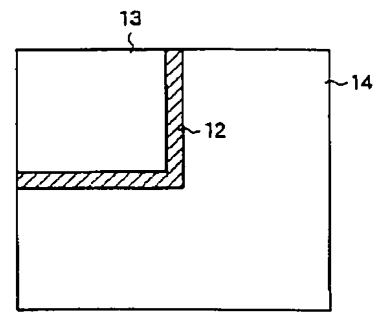
本発明の第１の実施形態の SOI 基板

【図２】



従来の半導体集積回路の製造工程

【図７】



本発明の第３の実施形態の SOI 基板

【図４】

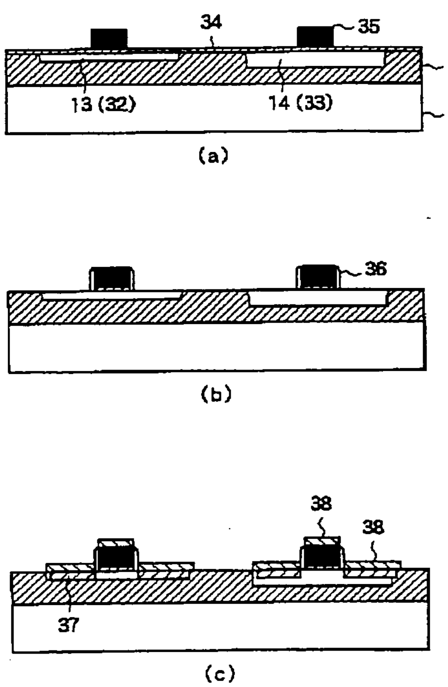
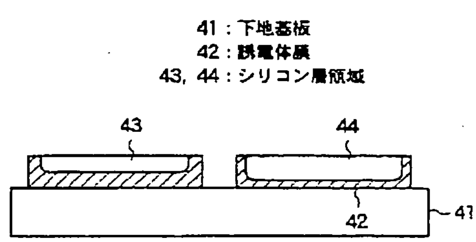


図１を用いた半導体集積回路の製造工程

【図５】



本発明の第２の実施形態の SOI 基板

【図３】

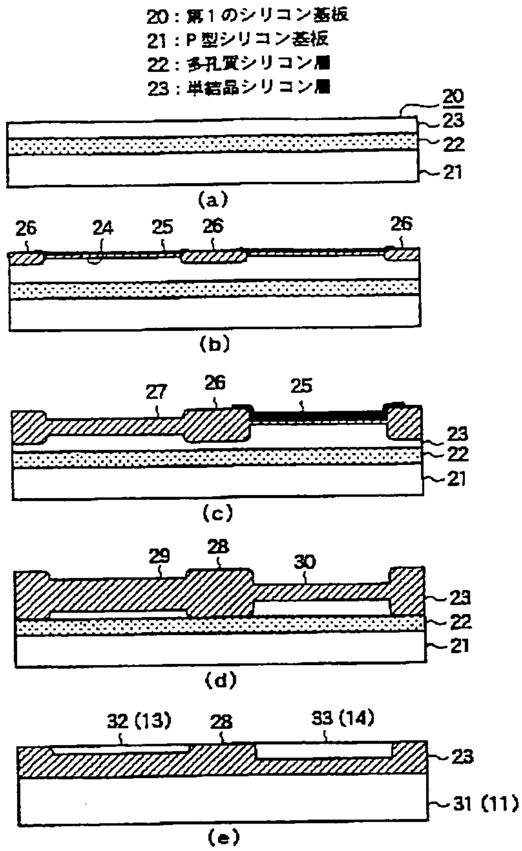


図１のSOI基板の製造工程

【図６】

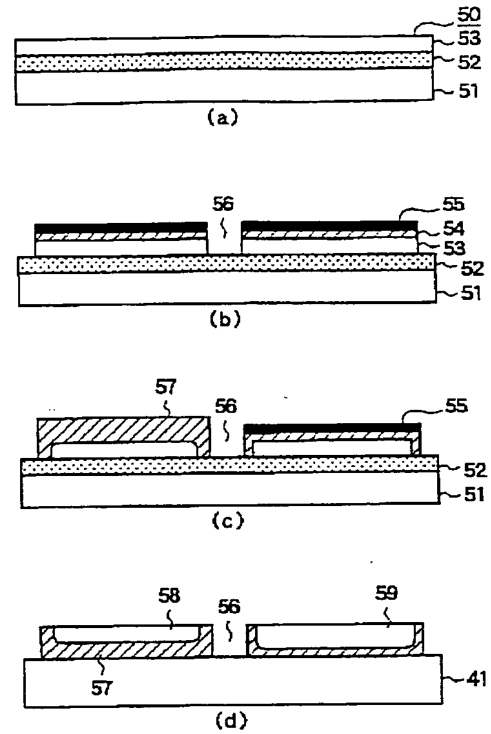


図５のSOI基板の製造工程

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